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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,581	07/22/2003	Isamu Kobori	07977-024003	6534

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FISH & RICHARDSON P.C.
1425 K STREET, N.W.
11TH FLOOR
WASHINGTON, DC 20005-3500

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/623,581	KOBORI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 7/22/03. Currently, claims 16-45 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 7/22/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The disclosure is objected to because of the following informalities: On page 12, lines 12-16, "silicon oxide film 407" and "gate electrodes 407" have the same reference number. On figure 4B, it appears that the reference number for the "silicon oxide film" should be "406". Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 37-45 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 28-36. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after

allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16, 17, 19, 22, 23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsumoto US Patent 5,396,084.

Matsumoto discloses the semiconductor method as claimed. See figures, 1-5, and corresponding text, where Matsumoto teaches, pertaining to claims 16 and 22, a method for forming an active matrix circuit comprising: doping a p-type impurity into a semiconductor layer **13** by ion doping to form a p-type impurity region **13b** in said semiconductor layer (figure 2C; col. 4, lines 18-34); activating said p-type impurity by annealing (col. 4, lines 30-34); and forming an interlayer insulating film comprising silicon nitride **19** (and silicon oxide layer **21**, claim 22) over said semiconductor layer (figure 1; col. 4, lines 65-68; col. 5, lines 6-21).

Pertaining to claims 17 and 23, Matsumoto teaches a method, wherein said active matrix circuit is incorporated into a liquid-crystal display (figure 5; col. 1, lines 5-10).

Pertaining to claims 19 and 25, Matsumoto teaches a method, wherein said active matrix circuit is incorporated into a liquid-crystal electro-optical device (figure 5; col. 1, lines 5-10

Note: it is inherent that a liquid-crystal electro-optical device is included as a type of liquid-crystal display device).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18, 20, 21, 24, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto US Patent 5,396,084 in view of Shannon US Patent 5,466,617.

Matsumoto discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 16, 17, 19, 22, 23 and 25 under 35 U.S.C. 102(b). In addition, Matsumoto shows, pertaining to claims 21 and 27, the method, further comprising crystallizing said amorphous island (see abstract).

However, Matsumoto fails to show, pertaining to claims 18 and 24, a method wherein said active matrix circuit is incorporated into an image sensor. In addition, Matsumoto fails to show, pertaining to claims 20 and 26, the method wherein said semiconductor layer comprises an amorphous semiconductor island having a plane area of 1000 μm^2 or less.

Shannon teaches, a similar method of forming an active matrix circuit that is incorporated into an image sensor (col. 9, lines 63-67; col. 10, lines 1-3).

It would have been obvious to one of ordinary skill in the art to incorporate, wherein said active matrix circuit is incorporated into an image sensor, pertaining to claims 18 and 24, in the

method of Matsumoto, according to the teachings of Shannon, with the motivation of creating a different electronic device that requires the use of a switching array (active matrix), for the purpose of controlling an array of image sensing devices.

It would have been obvious to one of ordinary skill in the art to incorporate, the method wherein said semiconductor layer comprises an amorphous semiconductor island having a plane area of 1000 μm^2 or less, pertaining to claims 20 and 26, in the method of Matsumoto, according to both the teachings of Matsumoto in view of Shannon, with the motivation that, the conventional active matrix circuits, taught by both Matsumoto and Shannon, generally include a plurality of thin film transistor devices used as a driving circuit, where these transistors are formed on semiconductor islands. For example, as stated in the abstract, Matsumoto teaches, forming a polysilicon island by crystallizing amorphous silicon film. Therefore, forming an amorphous semiconductor island having an area of 1000 μm^2 or less, would result in routine experimentation.

Claims 28, 29, 30, 31, 33-40 and 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto US Patent 5,396,084 in view of Iwanaga et al., US Patent 5, 932, 484.

Matsumoto discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 16, 17, 19, 22, 23 and 25 under 35 U.S.C. 102(b). In addition, Matsumoto shows, pertaining to claims 31 and 40, a method, wherein said active matrix circuit is incorporated into a liquid-crystal display (figure 5; col. 1, lines 5-10). Also, Matsumoto shows, pertaining to claims 33 and 42, a method, wherein said active matrix circuit is incorporated into a

liquid-crystal electro-optical device (figure 5; col. 1, lines 5-10 ***Note***: it is inherent that a liquid-crystal electro-optical device is included as a type of liquid-crystal display device). Finally, Matsumoto shows, pertaining to claims 35 and 44, a method, further comprising crystallizing said amorphous semiconductor island (see abstract).

However, Matsumoto fails to show, pertaining to claims 28 and 37, forming a conductive layer comprising titanium and an aluminum over said interlayer insulating film. In addition, Matsumoto fails to show, pertaining to claims 29 and 38, a method, wherein said conductive layer comprises an electrode. Also, Matsumoto fails to show, pertaining to claims 30 and 39, a method wherein said conductive layer comprises a wiring. Matsumoto fails to show, pertaining to claims 34 and 43, a method, wherein said semiconductor layer comprises an amorphous semiconductor island having a plane area of 1000 μm^2 or less. Finally, Matsumoto fails to show, pertaining to claims 36 and 45, a method wherein said titanium and said aluminum are formed in a multi-layer film.

Iwanaga teaches, on figures 7A-7E, and corresponding text, a similar method of forming an active matrix circuit, where titanium and aluminum layers are deposited on a interlayer dielectric through a contact hole, and patterned to form an interconnecting electrode (col. 11, lines 43-67; col. 12, lines 1-5).

It would have been obvious to one of ordinary skill in the art to incorporate, forming a conductive layer comprising titanium and an aluminum over said interlayer insulating film; a method, wherein said conductive layer comprises an electrode; a method wherein said conductive layer comprises a wiring; a method wherein said titanium and said aluminum are formed in a multi-layer film, pertaining to claims 28-30, 36-39 and 45, in the method of

Matsumoto, according to the teachings of Iwanaga, with the motivation of, forming an electrical contact to the source region of the thin film transistor device, for the purpose of creating a more efficient connection, resulting in an increased reduction of ohmic contact resistance.

It would have been obvious to one of ordinary skill in the art to incorporate, the method wherein said semiconductor layer comprises an amorphous semiconductor island having a plane area of 1000 μm^2 or less, pertaining to claims 34 and 43, in the method of Matsumoto, according to both the teachings of Matsumoto in view of Iwanaga, with the motivation that, the conventional active matrix circuits, taught by both Matsumoto and Iwanaga, generally include a plurality of thin film transistor devices used as a driving circuit, where these transistors are formed on semiconductor islands. For example, as stated in the abstract, Matsumoto teaches, forming a polysilicon island by crystallizing amorphous silicon film. Therefore, forming an amorphous semiconductor island having an area of 1000 μm^2 or less, would result in routine experimentation.

Claims 32 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto US Patent 5,396,084 in view of Iwanaga et al., US Patent 5932,484 in further view of Shannon US Patent 5,466,617.

Matsumoto in view of Iwanaga discloses the semiconductor substantially as claimed. See the preceding rejection of claims 28, 29, 30, 31, 33-40 and 42-45 under 35 U.S.C. 103(a).

However, Matsumoto in view of Iwanaga, fails to show, pertaining to claims 32 and 41, a method wherein said active matrix circuit is incorporated into an image sensor.

Shannon teaches, a similar method of forming an active matrix circuit that is incorporated into an image sensor (col. 9, lines 63-67; col. 10, lines 1-3).

It would have been obvious to one of ordinary skill in the art to incorporate, wherein said active matrix circuit is incorporated into an image sensor, pertaining to claims 32 and 41, in the method of Matsumoto in view of Iwanaga, according to the teachings of Shannon, with the motivation of creating a different electronic device that requires the use of a switching array (active matrix), for the purpose of controlling an array of image sensing devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Stanetta Isaac
Patent Examiner
January 31, 2005